

1 Introduction

1.1 Objectives

Astro is an integrated CEC targeted at the workstation market. Astro combines a memory controller and an IO controller on a single chip, using several smaller peripheral ASICs to control and drive the specific IO and memory buses (PCI, SDRAM).

The objective of this document is to describe the software interface to the Astro chip with enough detail to allow firmware and driver development. This ERS (along with referenced documents) contains enough information to ascertain the intended functionality of each block in Astro down to the register level.

1.2 Feature Summary

The following is a list of the major functionality in the Astro chip:

- 2GB/s peak memory BW
- Support for 125MHz SDRAM
- 125MHz turbo-mode Runway bus (250MT/s)
- 4GB max memory w/64Mb SDRAMs
- Low Memory Latency (13 cycles open page; 17 closed page)
- PCI 2.1 Compliance (w/Elroy)
- 8 I/O ropes for a high degree of I/O flexibility
- >1GB/s aggregate I/O Bandwidth
- 16-entry, fully associative I/O TLB
- 16-entry, fully associative coherent I/O buffer cache
- PDH Interface to the Dillon chip